Architecture Comprehensive Exam

Spring 2013

Student ID # _____

3/27/2013

The questions are on the attached page.
Write your answers on the paper provided.

Closed book, closed notes.
Calculators are not needed.

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1. Compare the benefits and disadvantages of RAID 1 with those of RAID 5. Make sure that you address performance, reliability and relative cost/per GigaByte.

2. The following questions refer to conditions that can occur during pipelining of instruction execution:

   a) Define the term *structural hazard* and describe how these hazards can occur and how they can be avoided.

   b) Describe how a *Read After Write* data hazard can occur and how they can be overcome.

   c) Many modern programming languages use *exceptions* to handle error conditions. Describe the impact of exceptions on pipelined execution and how certain characteristics of exceptions (synchronous vs. asynchronous or requested vs. coerced) affect the way that exceptions can be handled in the pipeline.

3. The following questions pertain to the memory cache on a single processor system:

    Given an 8 KByte instruction cache with a miss rate of 2% and an 8 KByte data cache with a miss rate of 5%, assume that 60% of the memory accesses are instruction references, that a cache hit takes 1 clock cycle, and a cache miss takes 25 clock cycles.

   a) What is the combined miss rate?

   b) What is the average memory access time?

   c) Explain the difference between a *write-through cache* policy and a *write-back cache* policy, including a brief description of the benefits of each.

   d) Describe two strategies for reducing the *miss rate* in caches.

4. Both of the following questions refer to dynamic scheduling techniques:

   a) Briefly explain how "scoreboarding" handles out of order execution.

   b) Describe the main differences between scoreboarding and the Tomasulo approach.

5. Both of the following questions refer to virtual memory:

   a) Briefly explain the benefits of using virtual memory in a multiuser computer system.

   b) Explain why a translation look-aside buffer (TLB) is used with virtual memory and describe how it improves the average memory access time.