

Architecture Comprehensive Exam

Spring 2014

Student ID # _____

3/18/2014

**The questions are on the attached page.
Write your answers on the paper provided.**

Closed book, closed notes.

Calculators are not to be used.

Architecture Comprehensive Exam - Spring 2014

1. In reference to **I/O systems**:
 - a) Define the terms **response time** and **throughput**.
 - b) Assume an I/O system in equilibrium, if the average time to service an I/O request is 40 ms and the I/O system averages 100 requests per second, what is the mean number of I/O requests in the system?
2. The following questions refer to conditions that can occur during **pipelining** of instruction execution:
 - a) Define the term **data hazard** and describe how these hazards can occur. Give an example of how two or more instructions can create a data hazard (you can use pseudocode or assembly language).
 - b) Describe how **forwarding** can be used to avoid data hazards. Use your example from part a) to explain how forwarding would solve that particular problem.
 - c) Explain how **branch prediction** is used to reduce the occurrence of pipeline hazards. Give an example that illustrates your explanation.
3. The following questions pertain to the **memory cache** on a single processor system:
 - a) Given a system with a cache hit time of 10ns, miss penalty of 100ns and hit rate of 95%, what is the average memory access time?
 - b) Explain the difference between a *write-through cache* policy and a *write-back cache* policy, including a brief description of the benefits of each.
 - c) Describe one advantage and one disadvantage of increasing the block size in a cache.
4. Both of the following questions refer to **virtual memory**:
 - a) Briefly explain the benefits of using virtual memory in a multiuser computer system.
 - b) Explain why a translation look-aside buffer (TLB) is used with virtual memory and describe how it improves the average memory access time.